R09

Code: 9A04504

B.Tech III Year I Semester (R09) Regular & Supplementary Examinations December 2014

DIGITAL IC APPLICATIONS

(Electronics and Communication Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Draw the transistor logic inverter circuit and analyze the circuit behavior with the help of transfer characteristics.

(b) Design CMOS transistor circuit for 2-input AND gate. Explain the circuit with the help of function table.

2 (a) Explain the following terms with reference to TTL gate:
(i) Logic levels.
(ii) DC Noise margin.
(iii) Low-state unit load.
(iv) High-state fan-out

(b) Design a transistor circuit of 2-input ECL NOR gate. Explain the operation with the help of function table.

3 (a) Explain data-flow design elements of VHDL.

(b) Design the logic circuit and write a data-flow style VHDL program for the following function:
(A) = $\Pi F_{P,Q,R,S}$ (1, 3, 4, 5, 6, 7, 9, 12, 13, 14)

4 (a) Write a process based VHDL program for the prime-number detector of 4-bit input and explain the flow using logic circuit.

b) (Explain data-flow design elements of VHDL.

5 ive the logic symbol for 74X138 and draw its logic diagram. Explain its operation with its truth table.

6 Write a VHDL code for 8 bit comparator circuit. Using this entity, write VHDL code for 32 bit comparator. Show the additional logic used for this purpose and use structural style of modeling.

7 Show the logic diagram of 74X175 IC and write VHDL code for it in data flow model. Using this entity, develop the program for 16 bit register and show the corresponding circuit and also explain how the register is cleared.

8 Draw the logic symbol and determine the size of a ROM that realizes an 8X8 combinational multiplier.

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